RC4559

Dual High-Gain Operational Amplifier

Features

- Unity gain bandwidth – 4.0 MHz
- Slew rate – 2.0 V/μS
- Low noise voltage – 1.4 μVRMS
- Supply voltage – ±22V for RM4559 and ±18V for RC4559
- No frequency compensation required
- No latch up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

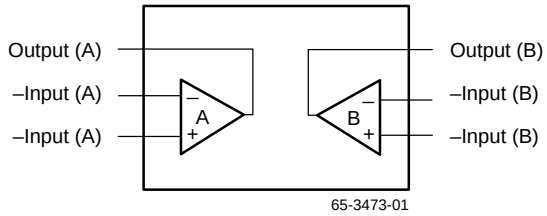
Description

The RC4559 integrated circuit is a high performance dual operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

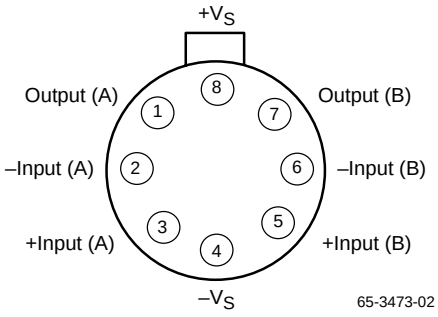
These amplifiers feature improved AC performance which far exceeds that of the 741-type amplifiers. The specially designed low-noise input transistors allow the RC4559 to be used in low-noise signal processing applications such as audio preamplifiers and signal conditioners.

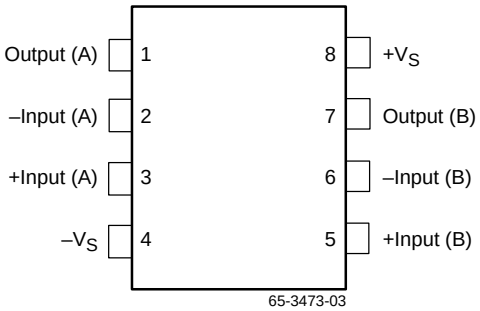
The RC4559 also has more output drive capability than 741-type amplifiers and can be used to drive a 600Ω load.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RM4559			±22	V
	RC4559			±18	
Input Voltage[2]				±15	V
Differential Input Voltage				30	V
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	
	CerDIP			833	
	TO-99			658	
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP, TO-99			175	
Operating Temperature	RM4559	-55		125	°C
	RC4559	0		70	
Lead Soldering Temperature	PDIP, CerDIP, T0-99 (60 sec)			300	°C
	SOIC (10 sec)			260	
Output Short Circuit Duration[3]		Indefinite			

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one op amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Typ	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

Parameters	Test Conditions	RM4559			RC4559			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	100		5.0	100	nA
Input Bias Current			40	250		40	250	nA
Input Resistance (Differential Mode)		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \ge 10k\Omega$	±12	±14		±12	±14		V
	$R_L \ge 2k\Omega$	±10	±13		±10	±13		
	$R_L \ge 600\Omega$	±9.5	±10		±9.5	±10		
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \le 10k\Omega$	80	100		80	100		dB
Power Supply Rejection Ratio	$R_S \le 10k\Omega$	82	100		82	100		dB
Supply Current	$R_L = \infty$		3.3	5.6		3.3	5.6	mA
Transient Response								
Rise Time	V_{IN} = 20 mV, R_L = 2kΩ		80			80		μS
Overshoot	$C_L \le 100pF$		35			35		%
Slew Rate		1.5	2.0		1.5	2.0		V/μS
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Power Bandwidth	$V_{OUT} = 20V_{p-p}$	24	32		24	32		kHz
Input Noise Voltage[1]	F=20Hz to 20kHz		1.4	5.0		1.4	5.0	μV_{RMS}
Input Noise Current	F=20Hz to 20kHz		25			25		pA_{RMS}
Channel Separation	Gain = 100, F = 10kHz, R_S = 1kΩ		90			90		dB
The following specifications apply for RM = -55°C ≤ T_A ≤ +125°C, RC = 0° ≤ T_A ≤ +70°C								
Input Offset Voltage	$R_S \le 10k\Omega$			6.0			7.5	mV
Input Offset Current				300			200	nA
Input Bias Current				500			300	nA
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \ge 2k\Omega$	±10			±10			V
Supply Current	$R_L = \infty$		4.0	6.6		4.0	6.6	mA

Note:

1. Sample tested only.

Typical Performance Characteristics

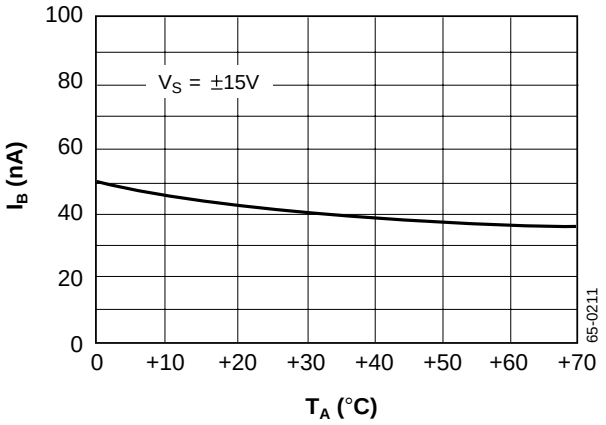


Figure 1. Input Bias Current vs. Temperature

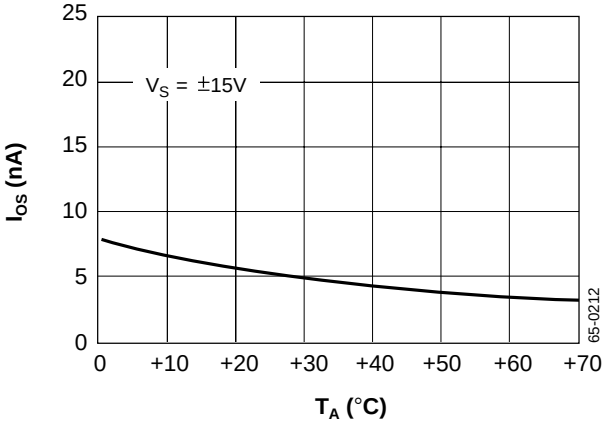


Figure 2. Input Offset Current vs. Temperature

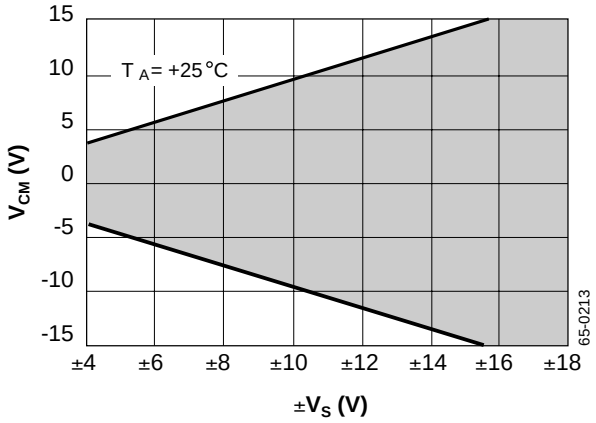


Figure 3. Input Common Mode Voltage Range vs. Supply Voltage

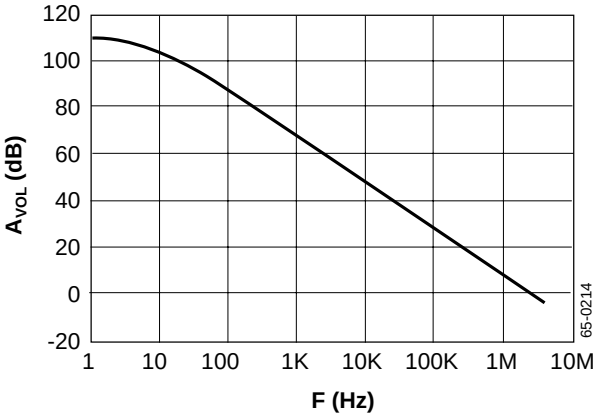


Figure 4. Open Loop Gain Voltage vs. Frequency

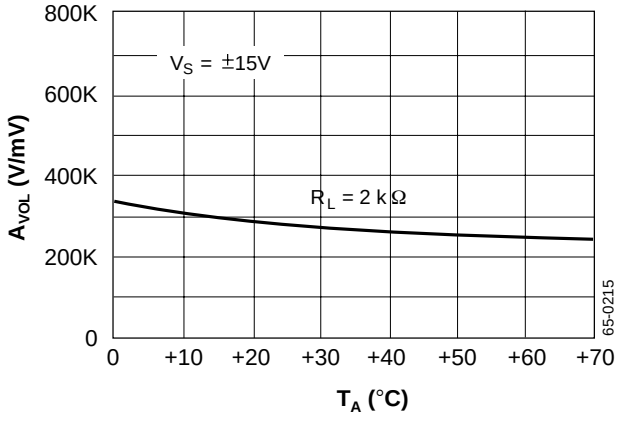


Figure 5. Open Loop Voltage Gain vs. Temperature

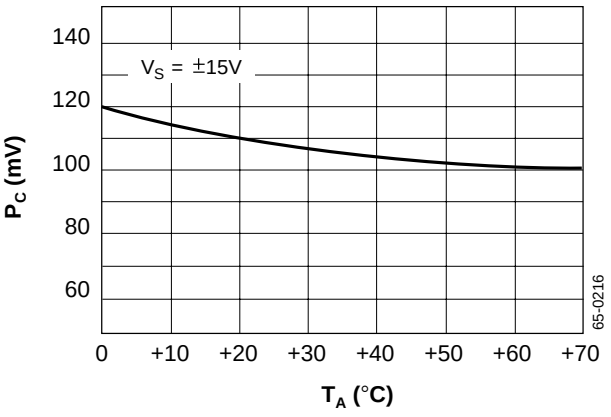


Figure 6. Power Consumption vs. Temperature

Typical Performance Characteristics (continued)

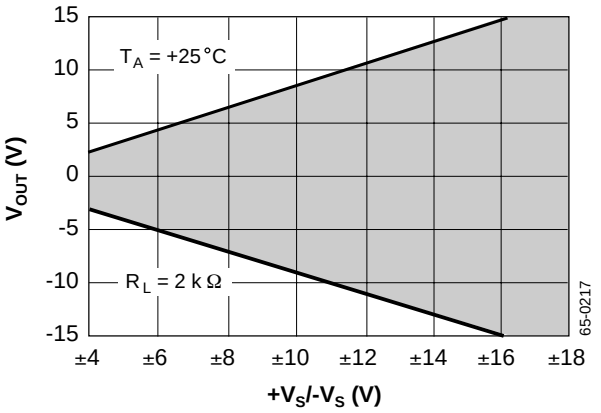


Figure 7. Output Voltage SWing vs. Supply Voltage

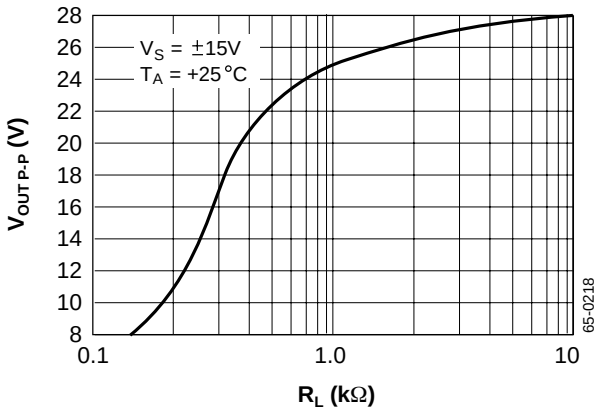


Figure 8. Output Voltage Swing vs. Load Resistance

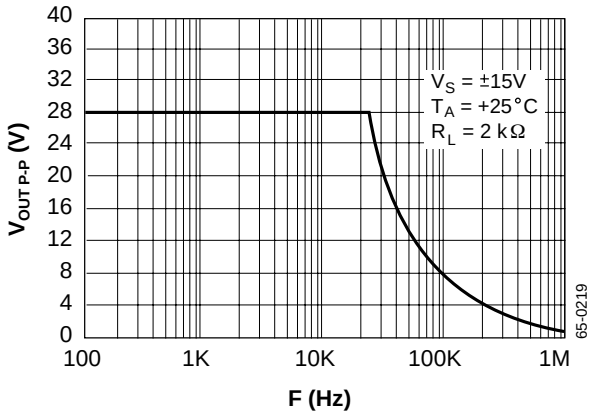


Figure 9. Output Voltage Swing vs. Frequency

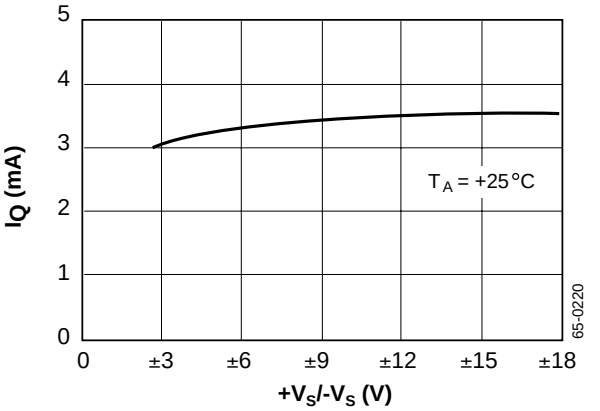


Figure 10. Quiescent Current vs. Supply Voltage

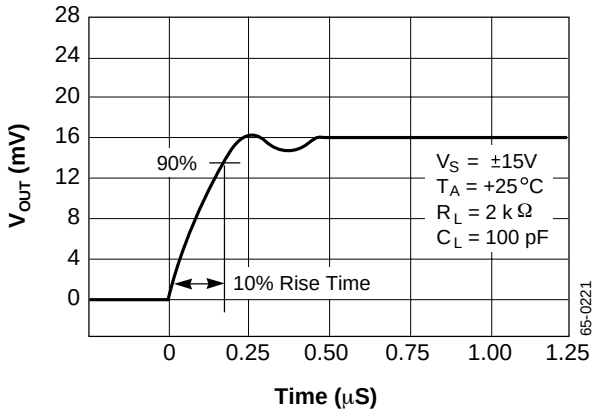


Figure 11. Transient Response Output Voltage vs. Time

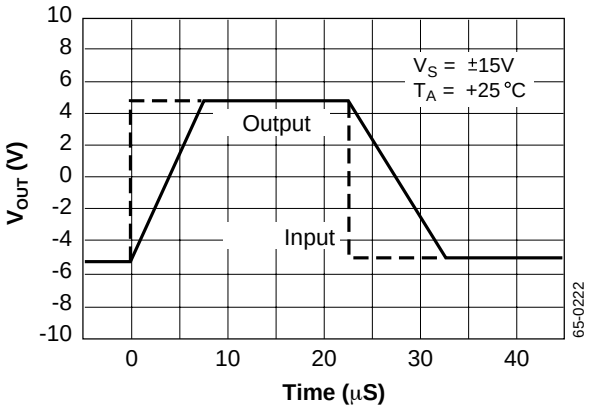


Figure 12. Follower Large Signal Pulse Response Output Voltage vs. Time

Typical Performance Characteristics (continued)

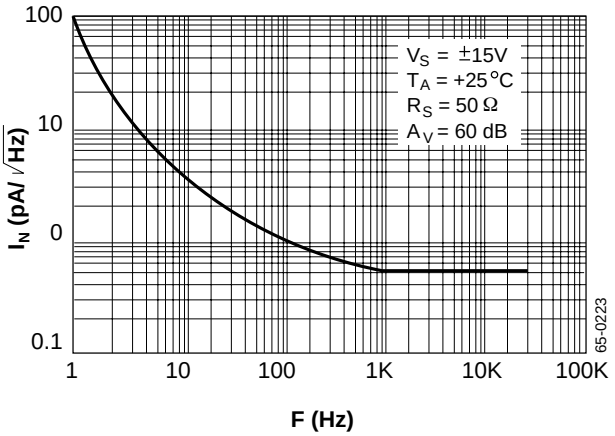


Figure 13. Input Noise Current Density vs. Frequency

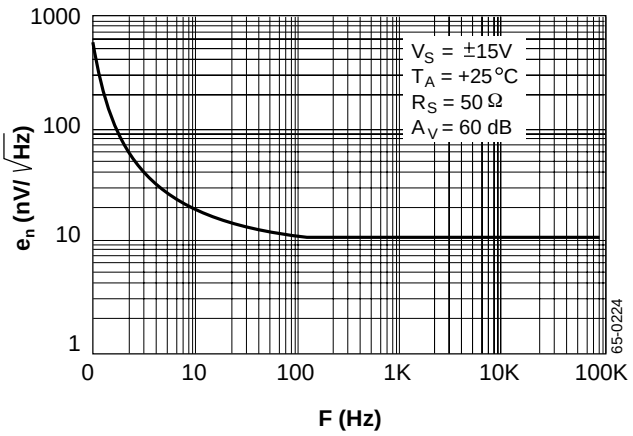


Figure 14. Input Noise Voltage Density vs. Frequency

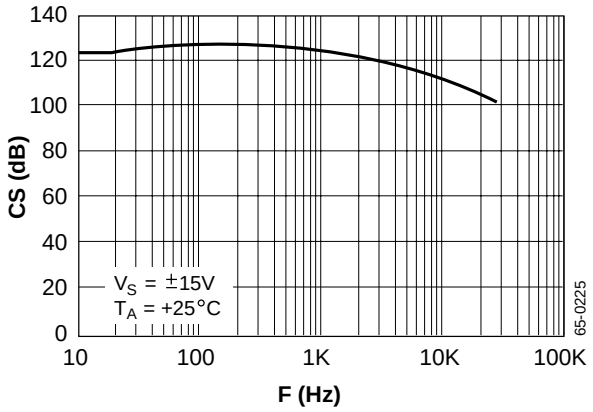


Figure 15. Channel Separation vs. Frequency

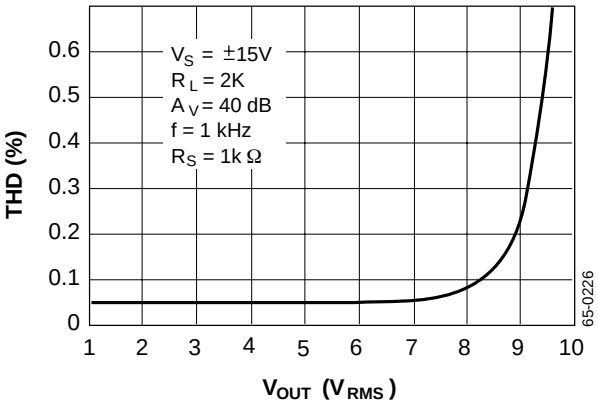


Figure 16. Total Harmonic Distortion vs. Output Voltage

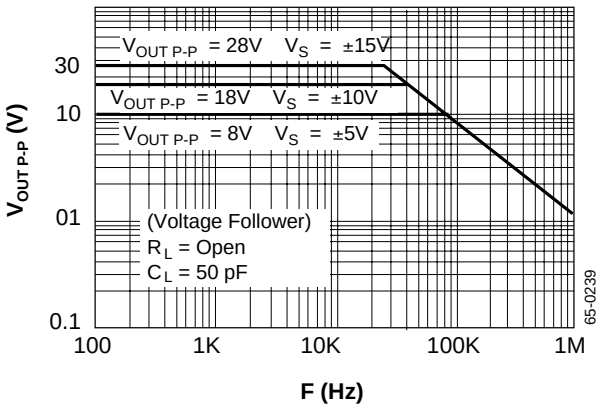


Figure 17. Output Voltage Swing vs. Frequency

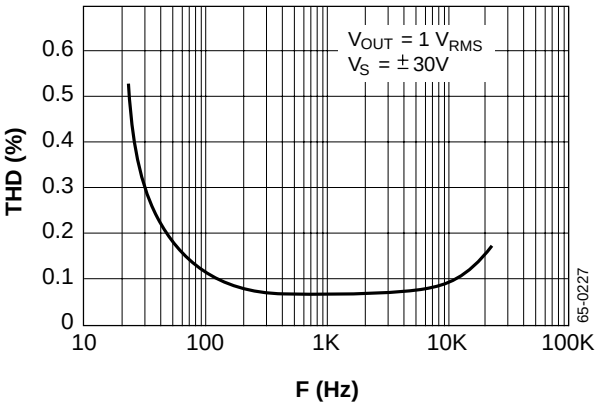


Figure 18. Distortion vs. Frequency

Typical Applications

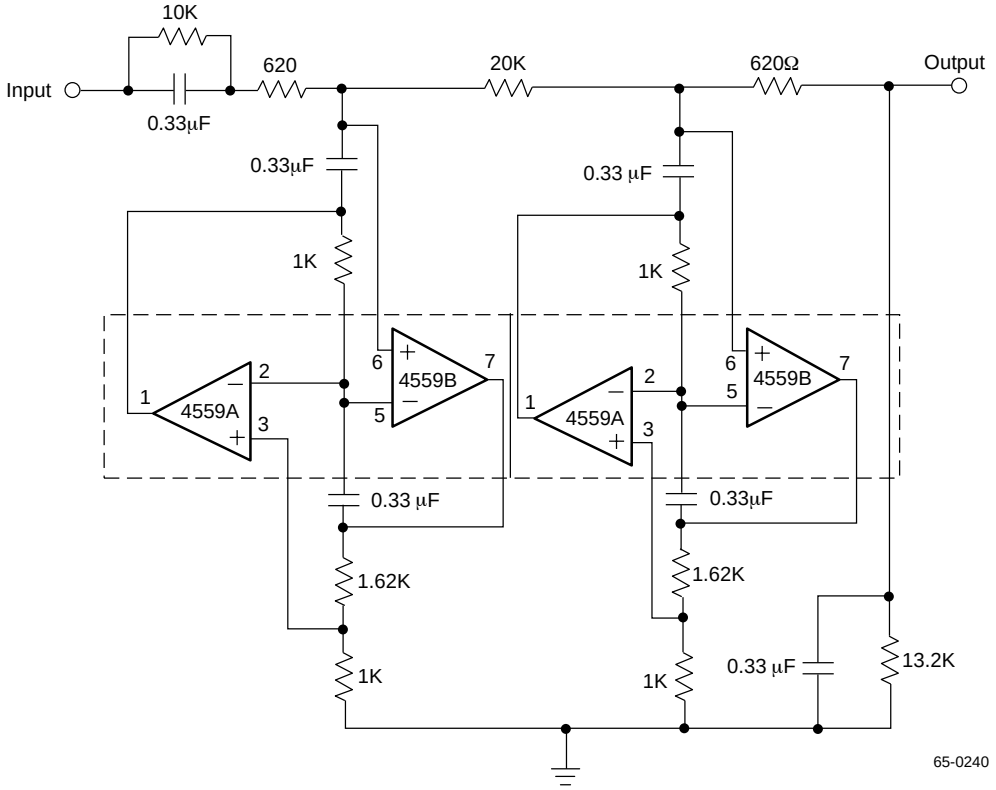


Figure 19. 400Hz Lowpass Butterworth Active Filter

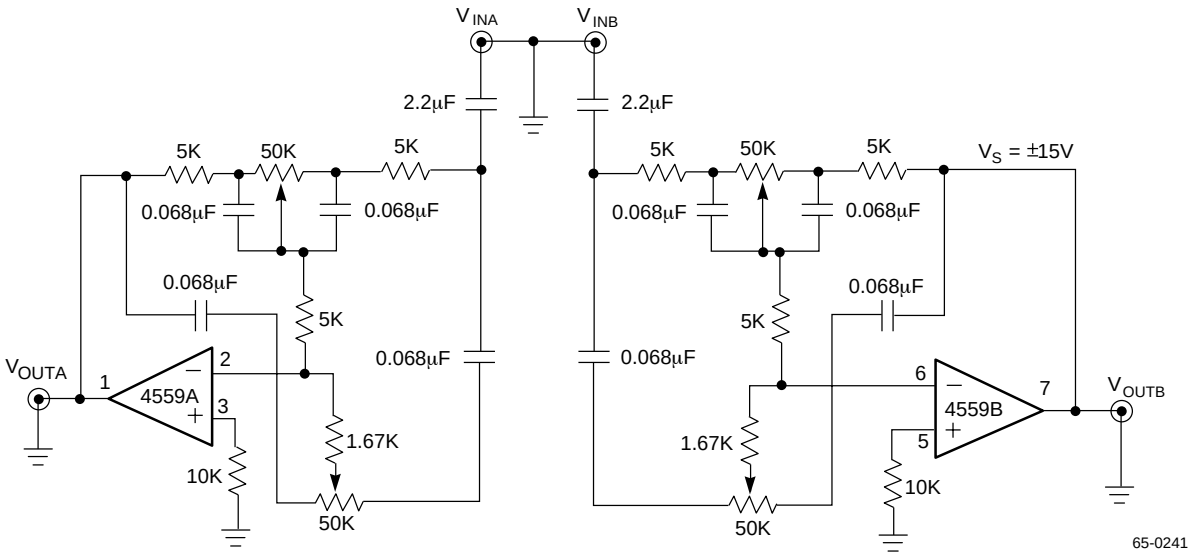


Figure 20. Stereo Tone Control

Typical Applications (continued)

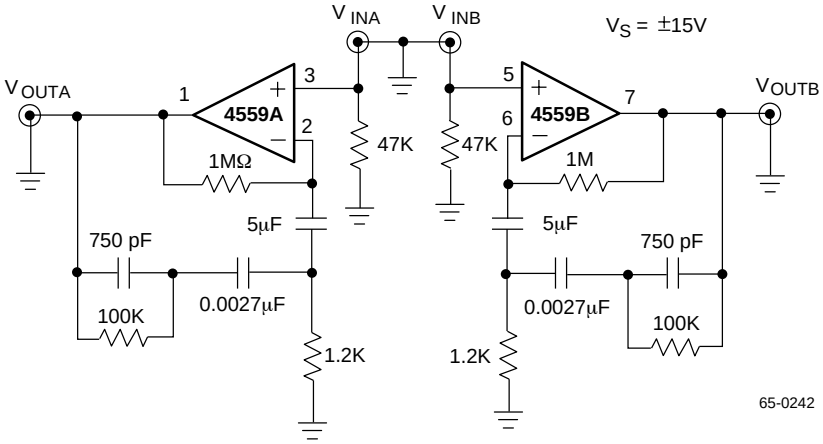


Figure 21. RIAA Preamplifier

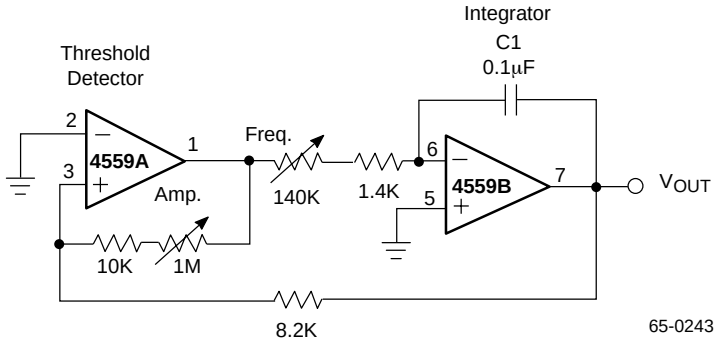


Figure 22. Triangular-Wave Generator

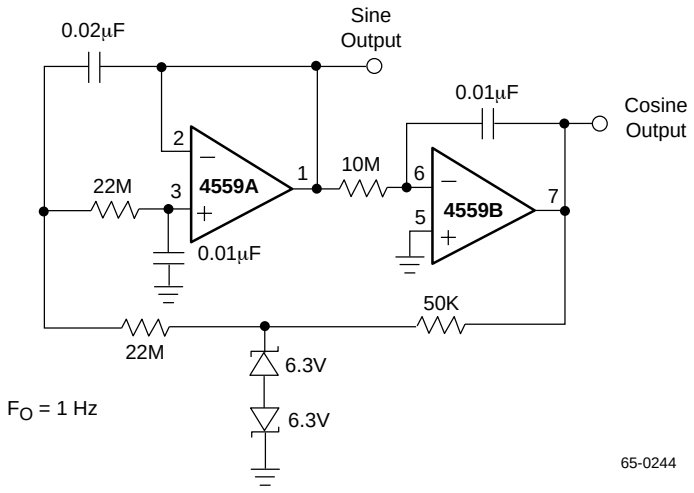
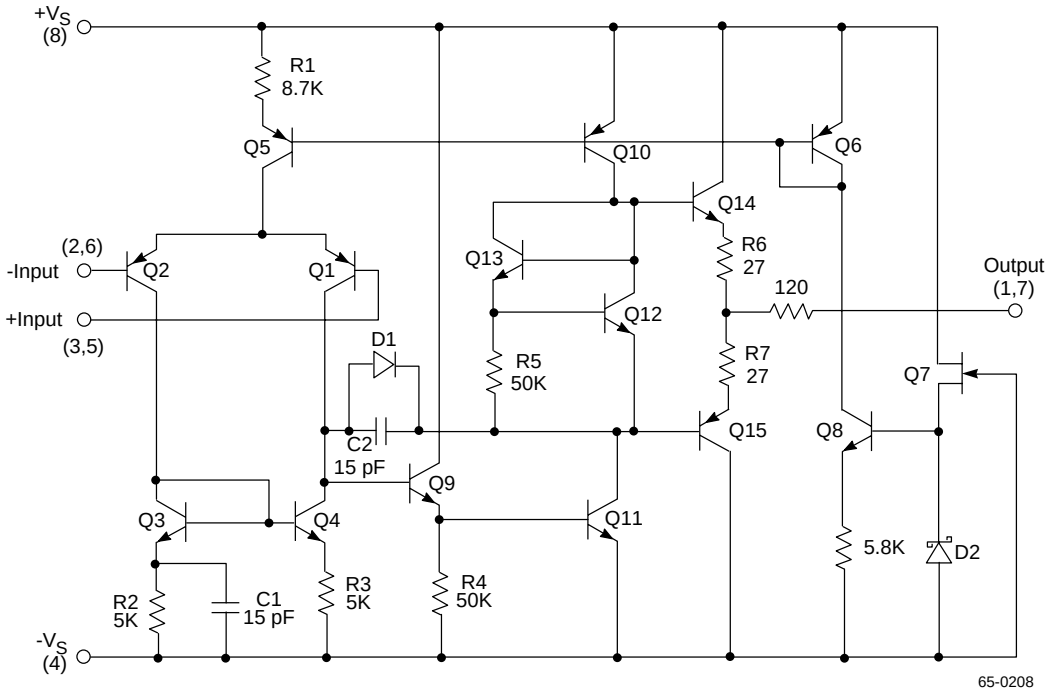


Figure 23. Low Frequency Sine Wave Generator with Quadrature Output

Simplified Schematic Diagram



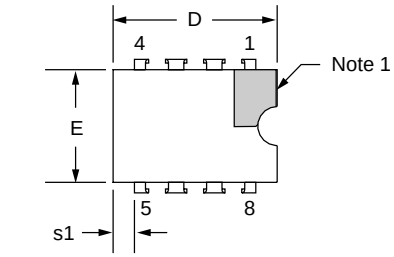
Mechanical Dimensions

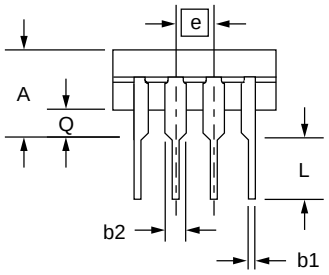
8-Lead Ceramic DIP Package

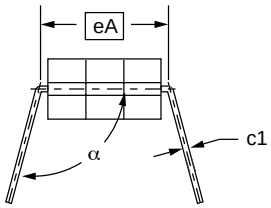
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







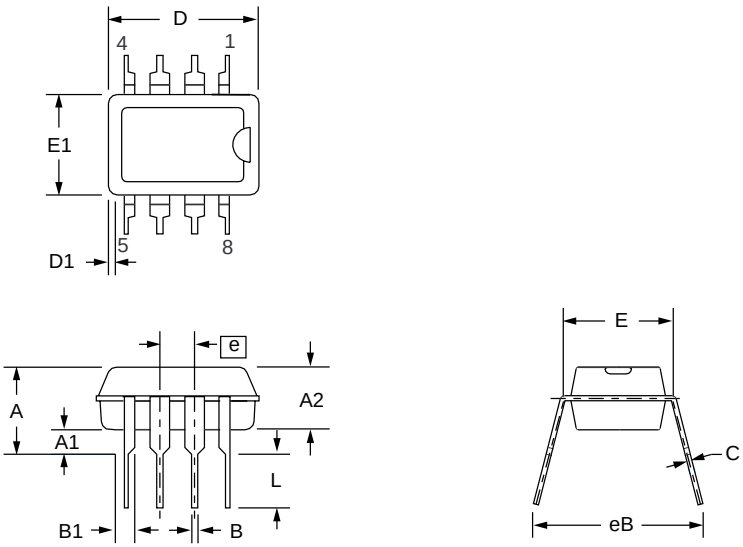
Mechanical Dimensions (continued)

8-Lead Plastic DIP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



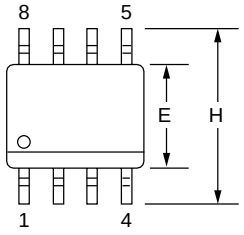
Mechanical Dimensions (continued)

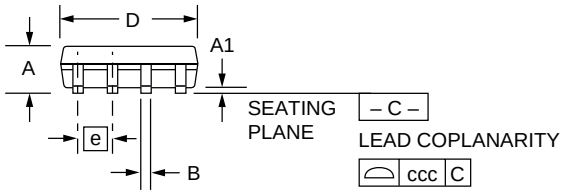
8-Lead SOIC Package

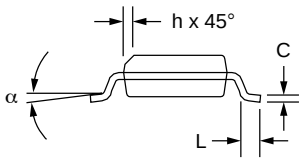
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.

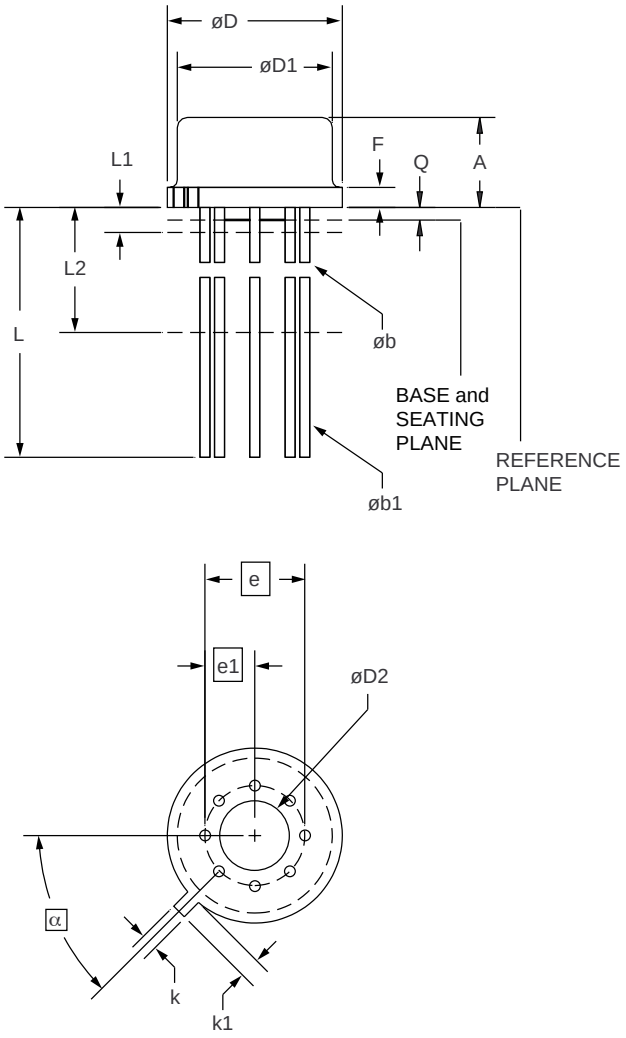






Mechanical Dimensions (continued)

8-Lead Metal Can IC Header Package



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

Ordering Information

Product Number	Temperature Range	Screening	Package
RC4559M	0° to 70°C	Commercial	8 Pin Wide SOIC
RC4559N	0° to 70°C	Commercial	8 Pin Plastic DIP
RC4559D	0° to 70°C	Commercial	8 Pin Ceramic DIP
RM4559D	-55°C to +125°C	Commercial	8 Pin Ceramic DIP
RM4559D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RM4559T	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM4559T/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

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